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Design of high-speed radar signal processor based on FPGA

Jinjin Xu[1,✉]

[1] *School of Electronics & Computer Science, University of Southampton, Southampton, Hampshire, SO17 1BJ, UK*

ABSTRACT

Radar ranging and speed measurement are common applications in daily life, with performance largely dependent on the radar signal processor. However, existing civilian radar signal processors struggle with weak signal reception and low analysis efficiency. This study designs a high-speed radar signal processor based on FPGA architecture, incorporating a fusion processing algorithm to integrate different radar signal bands, enhancing processing efficiency and accuracy. The design includes data feature analysis, storage, and fusion modules. Tests showed that the processor achieved real-time performance with a processing time under 1ms, a ranging error below 1m, and speed measurement accuracy within 5m/s, meeting practical requirements.

Keywords: high-speed radar signal, radar signal processor, field programmable gate array, processor design

1. Introduction

In terms of the radar working system, the phase-encoded radar technology solves the irreconcilable contradiction between the traditional radar system in terms of distance measurement and detection accuracy. At present, the more commonly used is two-phase coding (BPSK), that is, using two phase states to phase-modulate the carrier frequency signal. Therefore, the random coded signal is very suitable for the needs of today's radar waveform design, and it is also highly valued in the research of radar waveform design. The two working waveforms are transmitted simultaneously within the corresponding coherent accumulation time. The P-band radar receives the target echo after the end of the transmit pulse, and the D-band radar samples and processes the target beat echo during the valid period of the reception of the LFMCW transmit signal sweep period. The signal processor combines the echo signal processing results of P-band BPSK and D-band LFMCW to obtain accurate

✉ Corresponding author.
E-mail address: jx1n2024@163.com (J. Xu).

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distance and velocity measurement results of the target. However, high-speed radar signal processor has always been a problem that restricts the development of radar, so the research and design of high-speed radar signal processor based on FPGA in this paper is very necessary.

How to efficiently process radar signals has always been a hot topic of academic research. Coxson G E studied a radar signal processor sub-chain containing a pulse compression module employing binary phase codes to understand the behavior of output mean and variance as a function of phase code imbalance in noise-limited environments [2]. Klilou A proposed an efficient and scalable method for parallelizing the signal processing chain of pulsed Doppler radar [5]. Sugimoto Y compressed the SAR data by reconstructing the airborne image and extracting information from the reconstructed image, thus had solved the problem that radar feedback image recognition is not fast enough [14]. Sangston K J applied geometric intuition to the problem of radar signal processing, modeled and analyzed the transmission process of radar signals, and identified radar signals through the consumption and distance of radar propagation [20]. To resolve the sea clutter jamming signal, JRM F intensively processed 40 million computer-generated clutter power samples in MATLAB [9]. However, their improvements to the radar signal were only algorithmic improvements and did not make significant updates to the radar signal processor.

FPGA design is not a simple chip research, but mainly uses the FPGA model to design products in other industries. Molanes R F has performed extensive characterization and analysis of processor-FPGA communication in a widely used family of FPSoCs (i.e. Cyclone V devices) [10]. Sirkunan J proposed an HTM for embedded applications [12]. In order to reduce and speed up the design work, Laforest C E implemented an overlay architecture on the FPGA, which could achieve a faster construction of the FPGA architecture, but its performance and area costs were high [6]. Yoshimura C described an FPGA-based prototyping environment for developing the annealing processor architecture of the Ising model [17]. However, they payed more attention to the design of FPGA processors on the architectural aspect, and lacked the improvement on the application level.

In this paper, the software design of the P/D band composite high-speed stealth target detection radar signal processor was carried out on the hardware platform. Because the system has high requirements for real-time performance, in the process of algorithm implementation, the BPSK and LFMCW echo signal processing algorithms with large computational load were placed in FPGA with strong parallel computing capability. DSP mainly completed the fusion processing algorithm of BPSK and LFMCW signal processing results.

2. High-speed radar signal and algorithm

2.1. High-speed Radar

Linear Frequency Modulated Continuous Wave (LFMCW) radar is a radar system that acquires target information by transmitting electromagnetic waves whose frequency varies linearly with time. It has the characteristics of anti-stealth, strong anti-interference ability, high range resolution, no blind spot for distance detection, and good all-weather working ability [1]. There are many applications based on LFMCW radar, as shown in Figure 1.

The hardware system of P/D band composite high-speed stealth target detection radar consists of four parts: transmitter module, receiver module, local oscillator frequency source module and signal processing module. The signal processor controls the local oscillator frequency source to generate the P-band BPSK transmit signal and the P-band LFMCW signal required for the operation of the radar

system. The P-band BPSK transmission signal generated by the local oscillator frequency source is sent to the P-band transmitting module, and after being amplified by the transmitting module, it is sent to the P-band antenna to radiate into space. The P-band receiving module receives the BPSK echo signal reflected by the target, amplifies it, and sends it to the signal processor for AD sampling and processing. The transceiver switching between the P-band transmitting module and the receiving module is controlled by the signal processor through the corresponding interface. After the D-band LFMCW echo signal is received and de-skewed, an intermediate-frequency de-slope echo signal is generated and sent to the signal processor for AD sampling and signal processing [19, 8]. The working waveform of the P/D band radar is transmitted and received cooperatively during the detection process. The simple working principle is shown in Figure 2.

Fig. 1. LFMCW radar application

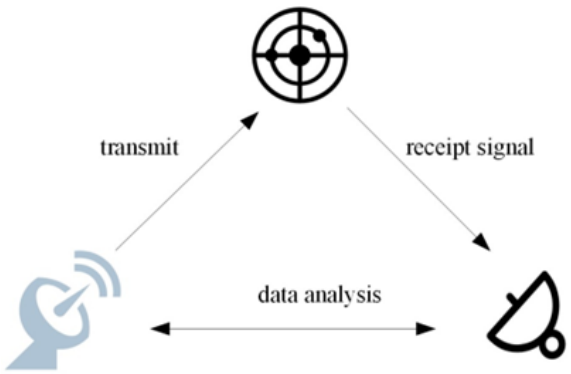


Fig. 2. Working principle of radar

2.2. FPGA software framework

The FPGA software framework of the signal processor consists of five parts, which are the waveform generation control module, the high-speed AD data interface module, the BPSK echo signal processing module, the LFMCW beat echo signal processing module and the data transmission module [7]. The overall design block diagram of the FPGA program is shown in Figure 3.

In the FPGA programming, the waveform generation control module is used to generate the synchronous timing signal and provide the timing required by the local oscillator frequency source to generate the transmit waveform, including the PRI signal and M-sequence symbol signal required

for the P-band BPSK signal, and the CPI signal and the frequency sweep signal required for the D-band LFMCW waveform [16].

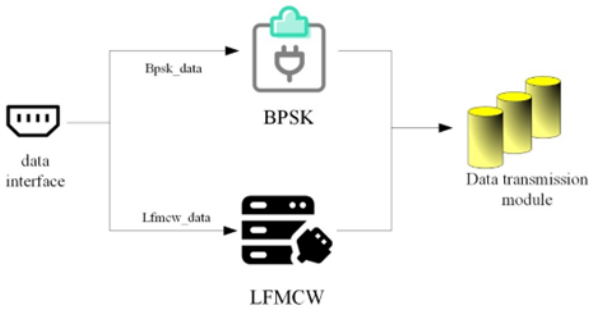


Fig. 3. FPGA structure

Regarding the high-speed AD data interface module, it is responsible for receiving and analyzing the serial data transmitted by two high-speed AD chips. Among them, the BPSK echo signal completes ADC sampling and digital down-conversion processing in the AD9680_1 chip, and the output data rate is 250MSPS. The LFMCW beat echo signal completes ADC sampling and digital down-conversion processing in the AD9680_2 chip, and the output data rate is 200MSPS. In the next step, the two echo signals are sent to the corresponding signal processing module for signal processing.

Regarding the BPSK echo signal processing module, the BPSK digital echo signal is correlated within the module at a symbol rate of 62.5MHz. After completing the related processing of a CPI, MTD processing is performed on the pulse pressure data of different distance gates, and then the MTD output is processed by CFAR for constant false alarm detection, and the target information is stored in the interface RAM of the data transmission module [18].

Regarding the LFMCW echo signal processing module, the digital beat echo signal enters the module for two-dimensional FFT processing. Perform 128-point FFT transformation in each frequency sweep cycle, and after one CPI (256 frequency sweep cycles), each corresponding distance gate performs 256-point FFT transformation in the second dimension. After the MTD processing is completed, a range-Doppler two-dimensional plane is formed, and the MTD results are sent to the CFAR sub-module for constant false alarm detection processing, and the target information is stored in the interface RAM of the data transmission module [15].

2.3. Design of radar signal fusion processing algorithm

2.3.1. P-band Signal. The expression of the P-band BPSK transmit signal is:

$$S_T(t) = a(t)e^{j\varphi(t)}e^{j2\pi f_0 t}. \tag{1}$$

The complex envelope of the signal is:

$$u(t) = a(t)e^{j\varphi(t)}. \tag{2}$$

Among them, f_0 is the carrier signal frequency and $\varphi(t)$ is the phase modulation function. For the BPSK signal, $\varphi(t)$ has two possible values of 0 and π, which can be represented by the binary phase sequence $\{\varphi_k = 0, \pi\}$ [4].

$a(t)$ is the window function that reflects the different waveforms emitted by the radar. For the BPSK waveform in the subject, the window function is a rectangular window, the width is the pulse

width, and has the following form in the duration of a transmit pulse:

$$a(t) = \begin{cases} 1; 0 < t < t_h = P\tau, \\ 0, eles. \end{cases} \tag{3}$$

Then the complex envelope of the BPSK signal can be written as:

$$u(t) = \begin{cases} \sum_{k=0}^{p-1} c_k v(t - k\tau); 0 < t < t_h, \\ 0, eles. \end{cases} \tag{4}$$

Among them, v(t) is the symbol waveform, τ is the symbol width, P is the code length, and $t_h = P\tau$ is the pulse width [3].

At time t_0, the target distance is R_0 and the relative velocity is v, then the echo delay is:

$$t_r = \frac{2(R_0 - vt)}{c} = \tau_0 - kt, \tag{5}$$

In Formula (5), c is the speed of light and τ_0 is:

$$\tau_0 = 2R_0/c. \tag{6}$$

Then the echo signal is:

$$S_r(t) = a(t - t_r)e^{j\varphi(t-t_r)}e^{j2\pi f_0(t-t_r)}. \tag{7}$$

Bring the echo delay into Formula (7), then the echo signal form is:

$$S_r(t) = K_r a(t - t_r)e^{j\varphi(t-t_r)}e^{j(2\pi(f_0+f_d)t-\varphi_0)}. \tag{8}$$

The carrier frequency signal is removed after mixing at the receiving end, and the expression of the echo signal is:

$$S_r(t) = K_r a(t - t_r)e^{j\varphi(t-t_r)}e^{j(2\pi f_d t-\varphi_0)} \tag{9}$$

Compared with the transmitted symbol signal, the echo baseband signal has two more parameters t_r, f_d, which reflect the distance and speed information of the target. The detection of the echo signal is mainly the detection of these two parameters [13].

2.3.2. D-band Signal. The working waveform of the D-band chirp continuous wave system radar is composed of M down-swept LFMCWs [11], as shown in Figure 4, where T_r is the frequency sweep period, M T_r is combined into a T_{CPI}, and T_{CPI} represents the coherent processing interval. A beat signal can be obtained after mixing the transmit waveform of each frequency sweep period with its echo signal, and the data of the consecutive M beat signals form a two-dimensional matrix.

The initial echo delay τ_m of the m-th down-sweep frequency band of the LFMCW multi-sweep cycle can be expressed as:

$$\tau_m = \frac{2(R - mvT_r)}{c} = \tau_0 - kmT_r \quad m = 0, 1, 2, \cdots, M - 1. \tag{10}$$

In general, the normalized Doppler frequency $k << 1$, the beat signal of the mth sweep period can be expressed as:

$$S_{B,n}^{-}(t) = 0.5K_r A_0^2 \cos[2\pi(\mu\tau_0 + f_d)t - 2\pi f_d T_r m) + \varphi]. \tag{11}$$

Among them, τ_0 represents the echo delay of the target at the beginning of the waveform, and φ represents the phase of the constant term.

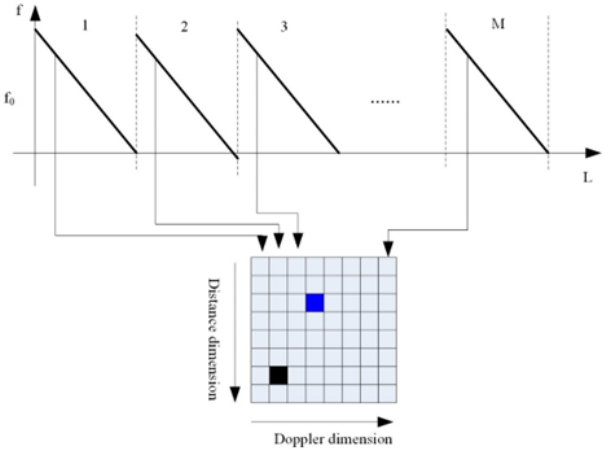


Fig. 4. Chirp CW + moving target detection system

It can be seen from Formula (12) that for the same target, the beat signal of each frequency sweep period has the same beat frequency:

$$f_B = \mu\tau_0 + f_d. \tag{12}$$

In addition, the initial phases of the beat signals between two adjacent frequency sweep periods differ by the same phase amount.

The beat frequency f_B of the distance dimension and the Doppler frequency f_d of the Doppler dimension satisfy:

$$\begin{cases} f_B = \mu\tau_0 + f_d, \\ f_d = \frac{2v_0 f_0}{c}. \end{cases} \tag{13}$$

By solving the binary first-order inequality, the distance and speed information of the target can be obtained:

$$\begin{cases} R_0 = \frac{(f_B - f_d)c}{2\mu}, \\ v_0 = \frac{cf_d}{2f_0}. \end{cases} \tag{14}$$

2.3.3. P/D band fusion signal. It can be seen from the simulation analysis of P-band and D-band radar signal processing that both the P-band BPSK working mode and the D-band LFMCW working mode have better ranging accuracy, so they can be used for target matching in the fusion process. In terms of speed measurement performance, the D-band LFMCW working mode has good speed measurement accuracy when the speed is less than the maximum unambiguous detection speed of the D-band. However, there is a problem that the speed measurement range of D-band radar is limited due to Doppler ambiguity, while the P-band BPSK working mode does not have speed measurement ambiguity, but has a large speed measurement error.

The P-band and D-band radar echo signal processing results are fused. The fusion processing process is shown in Figure 5.

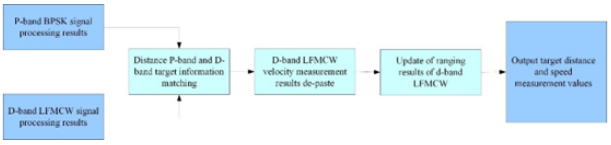


Fig. 5. P-band BPSK and D-band LFMCW signal processing results fusion processing

The specific steps are as:

Step 1: Match the detection results of the P-band and D-band in the distance dimension, and obtain the distance and velocity measurement results of the same target in the two working modes;

Step 2: For the same target, use the P-band radar speed measurement result v_p to determine the Doppler frequency measurement ambiguity multiple N_D of the target under the D-band radar, as shown in Formula (15) and Formula (16):

$$N_D = \left[\frac{v_p}{v_{\max,D}} \right], \tag{15}$$

$$v_{\max,D} = \frac{\lambda_D}{2T_{r,D}}. \tag{16}$$

Among them, $v_{\max,D}$ is the maximum unambiguous detection speed of the D-band LFMCW waveform.

Step 3: According to the obtained D-band Doppler frequency ambiguity multiple, perform deblurring processing to obtain the D-band unambiguous Doppler frequency f_d:

$$f_d = f_{d,D} + N_D / T_{r,D}. \tag{17}$$

Among them, $T_{r,D}$ is the sweep period of the D-band LFMCW waveform, and $f_{d,D}$ is the fuzzy Doppler frequency measured by the D-band radar.

The exact velocity of the target obtained from the unambiguous Doppler frequency f_d is:

$$v = \frac{f_d \lambda_D}{2}. \tag{18}$$

Among them, λ_D is the wavelength of the working waveform of the D-band radar LFMCW.

Step 4: Combine the D-band LFMCW target beat frequency with the unambiguous Doppler frequency to obtain the precise target distance as:

$$R = \frac{(f_B - f_d)c}{2\mu}. \tag{19}$$

Among them,

$$\mu = B_0 / T_{r,D}. \tag{20}$$

Formula (20) is the FM slope of the D-band LFMCW waveform.

2.4. Algorithm Simulation

In this paper, the simulation analysis combined the ranging and speed measurement performance of the processing algorithm. The fusion processing algorithm is to fuse the signal processing results of the same target under the P-band radar and the D-band radar. The target information is shown in Table 1.

Table 1. Target information

Target sequence number	Distance (m)	Radial velocity (m/s)
1	30	500
2	40	1500
3	50	2500

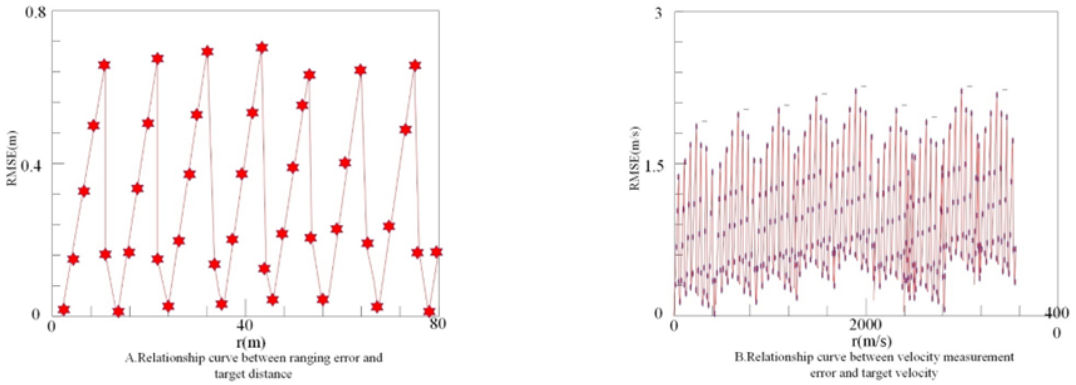
Table 2. Target detection result

Target sequence number	P band		D band		Fusion band	
	Distance (m)	velocity (m/s)	Distance (m)	velocity (m/s)	Distance (m)	velocity (m/s)
1	31.3	489.28	30.07	501.89	30.07	501.89
2	40.9	1465.84	40.12	543.02	39.6	1500.0
3	50.5	2442.5	51.08	587.87	50.1	2501.7

The processing results of the P-band BPSK echo signal and the D-band LFMCW echo signal and the calculation results after fusion processing are shown in Table 2.

It can be seen from the processing results in Table 2 that in terms of ranging performance, the P-band BPSK signal and the D-band LFMCW signal had good ranging accuracy, and were used for range-dimensional target pairing in fusion processing. In terms of speed measurement performance, P-band BPSK signal had low speed measurement accuracy and no speed measurement ambiguity, while D-band LFMCW speed measurement accuracy was high, but speed measurement ambiguity occurred. Through the speed de-blurring of fusion processing, the Doppler ambiguity multiple N_D of the target under the D-band radar can be obtained, and finally the precise distance and speed information of the target can be obtained.

Then, the distance measurement error and speed measurement error of the fusion processing algorithm in the entire detection distance and speed dynamic range were further analyzed. Figure 6a is a relationship curve between ranging error and target distance, and Figure 6b is a relationship curve between speed measurement error and target speed.



(a) VGG16 confusion matrix (b) VGG16 confusion matrix

Fig. 6. Error relationship curve

Through the analysis of Figure 6, it can be obtained that the ranging error of the P/D band composite detection radar was less than 1m, and the speed measurement accuracy was better than 3m/s. The fusion processing had good ranging accuracy and speed measurement accuracy in the entire dynamic range of ranging and speed measurement.

In this paper, the framework of the P/D band composite high-speed stealth target detection radar was given first, and then the working waveform design of the P-band BPSK radar and the D-band LFMCW radar was completed, and the ranging and speed measurement performance of the two radar working waveforms was simulation analyzed. From the simulation results, the P-band radar speed measurement was not ambiguous, but its speed measurement accuracy was poor; the D-band radar speed measurement accuracy was high, but it had the phenomenon of speed measurement ambiguity.

In order to achieve the purpose of high-precision ranging and speed measurement, the design of the P/D-band radar signal fusion processing algorithm was completed, that is, the Doppler deblurring of the D-band radar was performed using the unambiguous speed measurement results of the P-band radar. Finally, the feasibility of the fusion processing algorithm was verified by simulation analysis.

3. Design of high-speed radar signal processor

3.1. Radar signal processor hardware platform

Since the signal processor needs to realize the BPSK and LFMCW echo signal processing and logic control functions with high intermediate frequency and large bandwidth, the data rate is high and the real-time requirement is high. This requires the signal processor to have strong computing power, abundant storage resources and complex logic timing control capabilities. Therefore, the radar signal processor board circuit adopts the FPGA+DSP architecture, and the rational design and application of the DSP+FPGA architecture enables the signal processor to have better control flexibility and more efficient processing capabilities. The FPGA chip adopts the XC7VX690TFPGA of the VIRTEX-7 series of Xilinx Company, which has abundant logic units and storage resources, and has strong parallel computing capability. Therefore, the signal processing algorithm with a large amount of computation is implemented on the FPGA to meet the real-time requirements of radar. The DSP chip uses TI's high-performance multi-core floating-point DSPTMS320C6678, which has high-precision complex signal processing capabilities and is used for fusion processing of BPSK and LFMCW signal processing results.

3.2. Overall framework of signal processor software

The overall framework of the algorithm software implementation is shown in Figure 7:

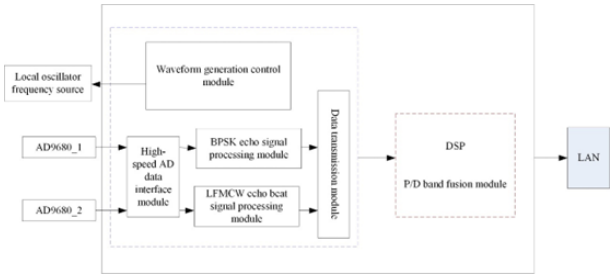


Fig. 7. Overall frame diagram of signal processor implementation

The specific realization of the algorithm adopts FPGA+DSP platform. FPGA and DSP cooperate to complete dual-channel AD data acquisition, digital down-conversion processing, BPSK echo signal processing, LFMCW echo signal processing, and fusion processing of the two modes of signal processing results. The division of labor between FPGA and DSP is as:

The FPGA first obtains two digital echo signals that have been sampled by AD and digitally down-converted through the AD interface. The digital echo signal of channel A is sent to the BPSK echo signal processing module for pulse pressure, MTD and CFAR processing, and the digital echo signal of channel B is sent to the LFMCW echo signal processing module for two-dimensional FFT and CFAR processing. Finally, the radar echo signal processing results of the two working modes are sent to the DSP through the SRIO interface of the data transmission module.

The DSP first reads the signal processing results of the two working modes in the FPGA through

the SRIO interface, completes the fusion processing of the echo signal processing results of the two modes, and sends the target information to the host computer through the network port.

3.3. P/D band signal fusion processing and data transmission module

The targets received in the P-band and D-band are first condensed. The function of target agglomeration processing is to combine the data of the same target on adjacent distance gates and speed gates to a point, and then condense the data into one target.

The range and velocity are calculated from the range unit and Doppler unit of the condensed P-band and D-band echo signal processing results. If the P-band detection distance R_p and the D-band detection distance R_D satisfy $|R_p - R_D| < 2.4m$, it is determined that the distance and speed measurement results in the two working modes belong to the same target, and target matching is completed. If the pairing is successful, solve the measurement ambiguity multiple N_D at the D-band Doppler frequency for the P-band velocity measurement result v_p of the same target. According to the Doppler frequency measurement ambiguity multiple N_D, the Doppler deblurring is performed, and the unambiguous Doppler frequency of the target in the D-band is obtained. Finally, according to the unambiguous Doppler frequency, the accurate ranging and speed measurement results of the target in the D-band are calculated. After the end, the D-band target count is decremented by one. If the D-band target count is not 0, the next D-band target ranging result and the P-band target ranging result are used for target pairing. When the D-band target count is 0, all the D-band target ranging results and the P-band target ranging results complete the information comparison, and the fusion processing of core 0 ends. Inter-core communication is carried out by means of IPC interruption, and core 7 is notified to frame the target result obtained by core 0, and the fusion result is sent to the host computer through the network port for interface display.

After the P-band and D-band echo signals are processed, send a GPIO interrupt to notify the DSP to read the processing results of the P-band and D-band echo signals. The number of signal processing thresholds is not fixed at different CPIs. If the target number of the current CPI signal processing threshold is less than the target number of the previous CPI, the data will overlap, so it is also necessary to transmit the target number to facilitate DSP identification.

The data length L represents the effective data length, that is, the length of DATA1∼DATAL, and the check digit data is the 32-bit result of accumulating the entire frame of data together with the frame identifier. The definitions of the three frame identifiers are shown in Table 3.

Table 3. Data identification definitions

Bit	content	describe
31:0	Frame_ID	frame typeRPI calculationCPI calculationwaveform
31:16	PRI_CNT	describe
15:0	CPI_CNT	frame typeRPI calculationCPI calculationwaveform
6:0	Waveform_Type	describe

After the P-band echo signal and the D-band beat echo signal complete the corresponding signal processing, the processing results are framed and stored in the interface RAM, and the signal processing completion flags BPSK_done and LFMCW_done are pulled high. After detecting the rising edge of the flag, send the corresponding GPIO interrupt to the DSP, and notify the DSP to read the signal processing result of the FPGA. The GPIO8 interrupt corresponds to reading the

P-band signal processing results, and the GPIO9 interrupt corresponds to reading the D-band signal processing results.

3.4. FPGA and DSP SRIO communication interface design and debugging

RapidIO is a low-latency, high-bandwidth, high-speed data transmission interface based on packet switching, which is mainly divided into serial and parallel technologies. SRIO is the abbreviation of Serial RapidIO, which is mainly used for internal interconnection of tightly coupled systems to support chip-to-chip and board-to-board communication. In this paper, the system was used to realize the communication interconnection between DSP and FPGA.

SRIO transmission is based on a request and response mechanism. The master device sends a request packet to the target device, and the target device generates a response packet and sends it back to the master device to complete the entire transmission. The main transmission methods supported by SRIO are direct IO/DMA and message passing. In this paper, the system used the direct IO/DMA transmission method, the signal processor DSP was used as the master device, and the FPGA was used as the slave device, which mainly realized the reading of high-speed data on the FPGA side by the DSP.

In this system, the SRIO initialization content and main parameter settings on the DSP side are as: the reference clock frequency is 312.5MHz, the port transmission mode is X4lane mode, the line rate of each lane is 5Gbps, the device ID on the DSP side is 0x00, and the output mode is direct IO/DMA mode. The FPGA side mainly calls the srio core SerialRapidIOGen24.0 to implement the SRIO interface module.

4. High-speed radar signal processor test

In order to further verify the processing performance of the P/D band composite high-speed target detection radar signal processor, the function test of the signal processor system was carried out in this paper, which mainly included two parts of the test. The first part verified the correctness of the processing results of the signal processor under the conditions of different distances and speeds of the target in the echo simulator environment; the second part verified whether the signal processor satisfies the real-time performance.

4.1. System test environment introduction and platform construction

The hardware composition and software design of the target echo simulator have been described. The echo simulator can simultaneously generate the BPSK intermediate frequency echo signal of the target under the P-band radar and the LFMCW beat echo intermediate frequency signal of the D-band radar. In order to better verify the real-time and correctness of the signal processor, the simulator outputs target echoes of different distances and speeds and sends them to the signal processor for processing, and records the ranging error and velocity measurement error of the signal processor under different conditions. In the simulator environment, it is only necessary to connect the signal processor and the target simulator. The connection diagram of the test system is shown in Figure 8.

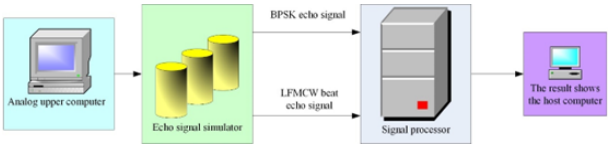
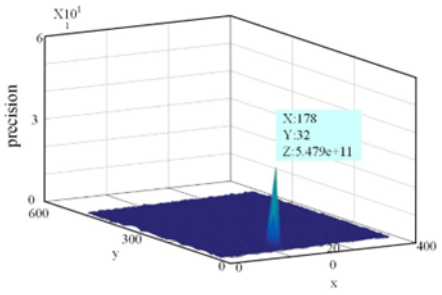


Fig. 8. Test system connection diagram

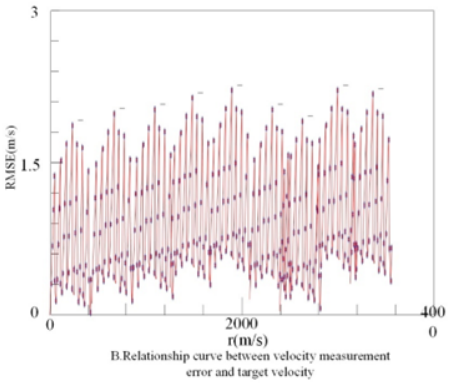
4.2. Signal processor functionality

After inputting the target distance and speed information of the two working waveforms on the host computer interface of the target simulator, open the debugging interface of the vivado software and the CCS software, and capture the processing results of the signal processor in the FPGA and DSP. The processing results of the signal processor in FPGA and DSP are as:

The FPGA extracts the BPSK digital baseband echo signal output by the AD, and performs pulse pressure processing at the symbol rate. Each range gate in the pulse pressure processing module obtains a correlation result after each PRI. The overall result is shown in Figure 9.



(a) Echo signal TMD result



(b) Incoherent accumulation result of direct wave signal

Fig. 9. Echo MTD processing and direct wave incoherent accumulation processing results

According to the test method, record the fusion processing results of the signal processor under the target conditions of different distances and different speeds. The test results are shown in Table 4.

Table 4. Fusion processing results

upper computer		Signal processing fusion result		Measuring accuracy (m)	Accuracy of speed measurement (m/s)
Distance (m)	velocity (m/s)	Distance (m)	velocity (m/s)		
1	150	1.68	149.52	0.68	-0.48
1	3000	1.28	2997.47	0.28	-2.53
25	150	25.12	149.56	0.12	-0.44
25	3000	25.48	2997.65	0.48	-2.45
55	150	54.85	149.58	-0.15	-0.42
55	3000	55.29	2997.84	0.29	-2.17
75	150	75	149.69	0	-0.31
75	3000	75.43	2997.97	-0.57	-2.03

4.3. Real-time performance of signal processor

To open the host computer interface of the target simulator, after setting the target distance and speed information, the two DDS chips of the simulator output the BPSK echo signal and the LFMCW beat echo signal respectively and send them to the signal processor. The signal processor performs real-time signal processing, and pulls out two signal lines through the TP test point on the signal processing board circuit. TP24 is the CPI reference signal, and TP25 is the GPIO14 signal. When the DSP is processing the P/D band signal fusion, GPIO14 outputs a high level. The level change of the TP test point detected by the oscilloscope is shown in Figure 10.

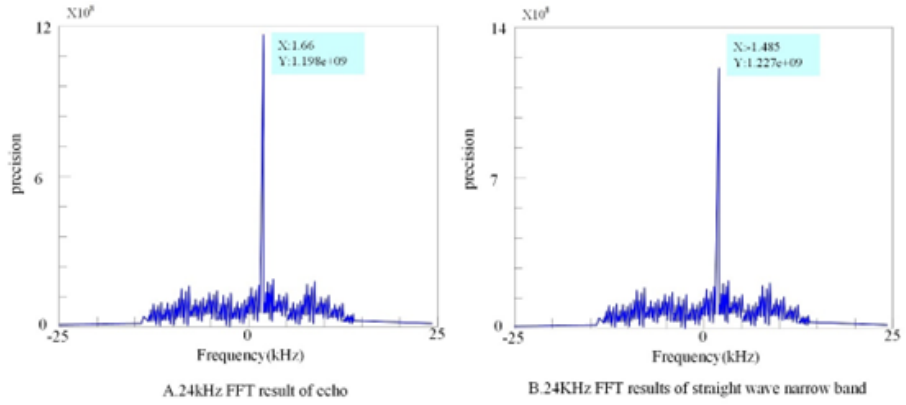


Fig. 10. FFT processing results of echo and live narrowband 24kHz data

As shown in Figure 10, the Figure 10A is the output of the TP24 test point of the signal processing board, and the CPI reference signal of the signal processor is recorded. The Figure 10B is the output of the TP25 test point of the signal processing board, which records the GPIO14 signal output by the signal processor DSP. When the DSP is processing the P/D band signal fusion, GPIO14 outputs a high level. As can be seen from the Figure 10, the system signal processing time is 916us, and the DSP processor completes the signal processing before the next CPI reference signal arrives. The system meets the real-time requirements and meets the index requirements.

5. Conclusions

At present, the radar signal processor adopts a dual-band radar composite detection system. The working waveforms of the two-band radars are transmitted and received cooperatively, while the D-band LFMCW system radar has a limited operating distance, and the P-band BPSK system radar has a long operating distance. In the future, it can be considered to apply the P-band radar to the target search at longer distances in the early stage, and then switch the working mode of the signal processor after detecting the target. This paper firstly introduced the FPGA architecture, and then studied the P/D fusion band signal algorithm. According to the algorithm principle, the processor module was designed. Finally, a brief introduction was made to the overall system and test environment of the P/D band composite high-speed target detection radar, and the real-time and functional performance of the radar signal processor was verified in the simulator environment. Although the overall experimental results have met the requirements, the radar signal processor has only been tested in the simulator environment, and then the detection performance test of the entire system needs to be carried out in the field environment.

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