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Intelligent Diagnosis of Integrated Circuit Short-Circuit Faults Based on Wavelet Neural Networks

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ABSTRACT
The smart diagnosis of included circuit (IC) quick-circuit faults is imperative on account of their capacity effect on digital structures' reliability and general overall performance. Those faults are inherently complex, posing vast traumatic situations in detection and prognosis. This paper introduces an modern diagnostic approach the usage of Wavelet Neural Networks (WNN), a sorting driven with the resource of WNN's skillability in signal processing. WNN's functionality to accurately deal with non-linear and non-desk bound indicators makes it especially appropriate for reading the difficult alerts related to IC faults. Our technique leverages the strengths of wavelet evaluation for characteristic extraction and neural networks for sample recognition, thereby enhancing fault analysis accuracy. The technique encompasses sign acquisition, preprocessing, feature extraction through wavelet transform, and type via a professional neural community. Comparative experiments with traditional techniques show off the proposed approach's superiority in phrases of accuracy and performance, underlining its capacity as a groundbreaking tool for IC fault analysis in advanced digital systems.

Keywords: Integrated Circuit Faults, Wavelet Neural Networks, Signal Processing, Feature Extraction, Fault Diagnosis

1. Introduction

Quick-circuit faults in integrated circuits (ICs) pose a quintessential venture inside the area of electronics [1]. Those faults can result in great performance degradation or whole failure of digital devices, emphasizing the importance of green and correct fault diagnosis. ICs, being the cornerstone of absolutely all contemporary electronic gadgets, have developed to end up fairly complex and densely packed with transistors [2-4]. This miniaturization, even as beneficial for performance and length reduction, amplifies the problem of detecting and diagnosing quick-circuit faults. Traditional

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techniques, in large part guide and time-consuming, are increasingly more insufficient as a result of the developing complexity of ICs [5-8]. Therefore, there is an urgent need for advanced, wise diagnostic techniques. Those methods have to not only cope with the tricky nature of cutting-edge ICs however additionally offer fast and reliable fault identity. This necessity drives the improvement of automatic and complicated diagnostic strategies, leveraging advancements in computing and machine mastering to meet the challenges posed by way of cutting-edge IC technologies [9].

Conventional techniques for diagnosing IC brief-circuit faults have numerous extensively, every with its own merits and limitations [10]. Early techniques were predominantly manual, which include visible inspections and simple electric testing, which have been hard work-intensive and error-inclined [11-12]. advancements brought about extra sophisticated strategies like electric signature analysis, which stepped forward reliability however still lacked the finesse to cope with increasingly complicated IC architectures [13]. Techniques which include Voltage comparison in Scanning Electron Microscopy supplied particular fault localization however were confined through their invasive nature and excessive operational fees [14]. Infrared Thermal Imaging emerged as a non-invasive opportunity, taking into account the detection of faults thru thermal anomalies. Different exceptional strategies consist of using Time-area Reflectometry, which provided more desirable fault detection capabilities [15-18]. Every of these strategies contributed to the understanding and development of IC fault analysis however also highlighted the want for greater advanced, integrated answers able to addressing the multifaceted nature of IC faults [19].

The integration of machine gaining knowledge of into IC fault prognosis represents a huge development in addressing the complexities of cutting-edge ICs [20]. Studies in this area has delivered numerous gadget learning-primarily based tactics, each demonstrating particular strengths and boundaries. Strategies making use of supervised learning algorithms, together with guide Vector Machines (SVM) and Neural Networks, have shown promise in as it should be classifying faults primarily based on pre-categorized facts [21]. Unsupervised learning strategies, like clustering, have been effective in identifying novel fault styles besides prior expertise. Deep gaining knowledge of models, in particular Convolutional Neural Networks (CNN), have excelled in extracting intricate features from complicated IC datasets, leading to more desirable diagnostic accuracy [22-23]. Ensemble techniques, combining multiple gadget learning fashions, have also been explored to enhance fault diagnosis robustness [24]. While these device getting to know-based strategies provide considerable improvements over conventional techniques, demanding situations such as information scarcity, version overfitting, and the want for huge training data persist. Despite the fact that, the ongoing evolution of system gaining knowledge of algorithms and their utility in IC fault analysis holds remarkable potential for revolutionizing the sphere.

Neural networks and their versions were notably studied for fault analysis in numerous domain names, along with incorporated circuits (ICs) [25]. A large frame of literature has explored using traditional neural networks, demonstrating their efficacy in pattern popularity and type duties. CNN, regarded for their powerful function extraction competencies, had been particularly effective in diagnosing complex IC faults. Recurrent Neural Networks (RNNs), with their capacity to system sequential records, have proven potential in temporal fault analysis [26]. Using Deep belief Networks (DBNs) has additionally been suggested, leveraging their deep architecture for greater nuanced fault detection. Additionally, Autoencoders had been hired for unsupervised anomaly detection in ICs, highlighting their utility in identifying unusual patterns indicative of faults [27-29]. The overarching advantage of these neural network-based tactics lies of their potential to research and adapt to the complex styles of IC faults, offering a high diploma of accuracy and efficiency in fault diagnosis [30-32].

Building upon the foundational work in neural networks for fault diagnosis, this paper explores the radical application of Wavelet Neural Networks (WNN) [33-34] for clever analysis of IC quick-circuit faults (WNN-ICFD). The incentive in the back of this technique stems from the need to beautify diagnostic accuracy and performance, addressing the demanding situations posed by using the complex nature of present day ICs. WNN combines the multi-decision evaluation power of wavelet transforms with the adaptive gaining knowledge of functionality of neural networks. This integration allows for powerful function extraction from non-linear and non-desk bound IC fault signals, which can be often challenging to analyze the use of conventional methods. The specific steps of our methodology encompass sign preprocessing, feature extraction thru wavelet evaluation, and classification the usage of a finely tuned neural network. Experimental results are offered to illustrate the efficacy of the proposed technique in as it should be diagnosing IC short-circuit faults. The innovative aggregate of wavelet analysis and neural networks marks a extensive development within the area of IC fault prognosis.

This look at contributes to the sphere of IC fault prognosis in 3 tremendous ways. Firstly, it introduces the software of Wavelet Neural Networks for IC short-circuit fault analysis, a novel technique that complements diagnostic accuracy and efficiency. Secondly, the paper demonstrates the effectiveness of mixing wavelet analysis with neural network-based learning, providing a robust solution for analyzing complicated fault alerts. Eventually, the empirical outcomes validate the prevalence of the proposed technique over conventional diagnostic strategies, showcasing its capability as a sensible tool for superior IC fault evaluation. Those contributions characterize a leap forward inside the smart diagnosis of IC faults, paving the method for more dependable and efficient digital structures.

2. WNN-ICFD

The proposed WNN-ICFD (Wavelet Neural community for included Circuit Fault analysis) technique is a comprehensive method designed for the green and correct diagnosis of short-circuit faults in incorporated circuits. This technique encompasses several key steps: data acquisition, sign preprocessing, function extraction through wavelet transform, and type the usage of a skilled neural community. Each stage performs a fundamental function in ensuring the general effectiveness of the fault analysis system. Initially, the information acquisition section involves accumulating electrical alerts from ICs, which might also contain indicative styles of capability faults. The signal preprocessing step is geared toward noise discount and normalization, making prepared the statistics for subsequent evaluation. Feature extraction is finished the use of wavelet remodel, a effective tool for decomposing indicators into components that capture every time and frequency data. Ultimately, a neural community is educated to classify the extracted features into fault categories, leveraging its capability to parent complex patterns.

2.1 Data Acquisition and Preprocessing

To start with, acquire uncooked sign records from integrated circuits.

$$X = \{x_1, x_2, \cdots, x_n\} \tag{1}$$

Each x_i is a discrete signal capturing various operational states and potential fault conditions in ICs.

Then, apply preprocessing techniques to the raw data X for noise reduction and normalization.

$$X_{pre} = f_{pre}(X) \tag{2}$$

$$f_{pre}(x) = \frac{x-\mu}{\sigma} \tag{3}$$

where μ and σ are the mean and standard deviation of X, respectively. This step is crucial for standardizing the data, ensuring consistency in signal magnitude across the dataset.

2.2 Feature Extraction Using Wavelet Transform

The preprocessed data X_{pre} is subjected to a wavelet transform to decompose the signals into their frequency and time-based components.

$$W = wavelet\_transform\left(X_{pre}\right) \tag{4}$$

The set of wavelet coefficients extracted from the signal, where each w_i represents a feature extracted from the signal, capturing both time and frequency information crucial for fault diagnosis.

$$W = \left\{w_1, w_2, \cdots, w_n\right\} \tag{5}$$

Specifically

$$w_i = \sum\nolimits_k x_k \psi_{i,k} \tag{6}$$

where $\psi_{i,k}$ are the wavelet basis functions and x_k are the signal samples. This transformation captures both frequency and time characteristics of the signal, essential for identifying intricate fault patterns in ICs.

2.3 Classification Using Neural Network

Enter Layer: The enter to the neural network is the set of wavelet-converted features W.

Hidden Layers: those layers perform the non-linearmodifications ofthe inputs. The wide variety of hidden layers and the quantity of neurons in every layer are hyperparameters that can be tuned based totally at the complexity ofthe statistics.

Output Layer: The output layer corresponds to the fault classes. If there are C fault categories, theoutputlayerwillhave C neurons.

Activation Function: Each neuron in the neural network uses an activation function, like ReLU or sigmoid, to introduce non-linearity into the model.

$$sigmoid = \frac{1}{1+e^{-x}} \tag{7}$$

$$ReLU = \begin{cases} x & if x \geq 0 \\ 0 & if x < 0 \end{cases} \tag{8}$$

The neural network N takes the wavelet features W as input and outputs the predicted labels $\hat{Y}$.

Loss Function: The commonly used loss function for classification tasks is Cross-Entropy Loss, represented as

$$L = -\sum\nolimits_{c=1}^{c} y_{o,c} \log\left(p_{o,c}\right) \tag{9}$$

where $y_{o,c}$ is a binary indicator of whether class label c is the correct classification for observation o and $p_{o,c}$ is the predicted probability of observation o being of class c.

Parameter Update: Parameters (weights and biases) of the neural network are updated using optimization algorithms like Stochastic Gradient Descent or Adam. The update rule is

$$\theta = \theta - \eta \nabla_\theta L \tag{10}$$

where θ represents the parameters, η is the learning rate, and $\nabla_\theta L$ is the gradient of the loss function with respect to the parameters.

The WNN-ICFD approach integrates wavelet transform with neural network analysis to diagnose short-circuit faults in integrated circuits. This technique leverages the wavelet remodel for its exceptional time-frequency sign decomposition and neural networks for their sturdy sample popularity and class abilities. The mixture of those 2 strategies enables a extra correct and green prognosis of complex fault patterns in ICs. The structure of WNN-ICFD is proven in Figure 1.

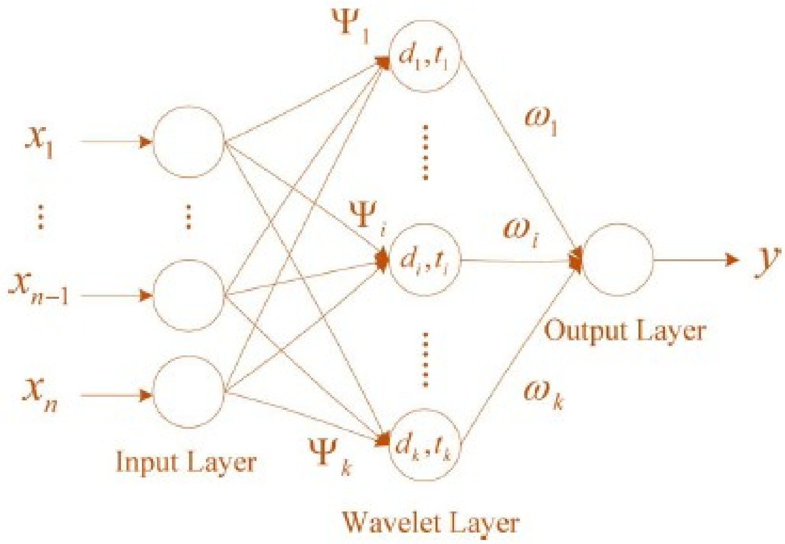

Fig. 1. The architecture of WNN-ICFD

3. Experiment Results

3.1 Experimental Setup

On this segment, we present the experimental evaluation of our proposed WNN-ICFD approach. Our experiments are designed to thoroughly assess the effectiveness o f WNN-ICFD in diagnosing short-circuit faults in integrated circuits. We evaluate the overall performance of WNN-ICFD against several set up machine mastering algorithms, which include help Vector system (SVM), Random woodland (RF), Convolutional Neural network (CNN), and a preferred Neural community (NN). The evaluation is conducted on 2 awesome datasets: a publicly available integrated Circuit Fault dataset (PD-ICF) and a synthetically generated dataset (SD-ICF), which collectively offera complete variety offault eventualities. We assess the techniques primarily based on key metrics including Accuracy, Precision, Recall, and F1 ratingtooffer aholistic viewof their performance in fault diagnosis.

Dataset Description

Public Dataset (PD-ICF): This dataset consists of real-world IC fault data accumulated from numerous publiclyto be had assets. It carries an inequality of fault scenarios, along with short-circuit situations, with annotated fault kinds and sign characteristics [15, 33].

Synthetic Dataset (SD-ICF): The synthetic dataset was once meticulously created to simulate a various varietyof IC fault situations no longer protected within the public dataset. This dataset involves:

1) Generating signals using digital circuit simulation software program to mimic the operational states of ICs.
2) Introducing faults, such as brief-circuit conditions, by means of changing circuit parameters.
3) Recording the consequent signals and annotating them with the corresponding fault types.

WNN-ICFD version Parameters displayed in a tabular formatfor clarity (Table 1):

Table 1. Parameters pf WNN-ICFD

Parameter	Value	Description
Hidden Layers	2	Twolayersinthe neural network
Neurons per Hidden Layer	64	Number of neurons in each hidden layer

Activation Function	ReLU, Softmax	ReLU in hidden layers, Softmax in output layer
WaveletType	Daubechies-4	Used forwavelet transform
Optimizer	Adam	Optimization algorithm for training
Learning Rate	0.001	Stepsizeat eachiterationof learning
Batch Size	32	Numberofsamplesperbatchintraining

Comparison Algorithms

Support Vector Machine (SVM): Known for its effectiveness in classification tasks, SVM is used to classify IC faults by finding the optimal hyperplane in a high-dimensional space [19].

Random Forest (RF): An ensemble method that uses multiple decision trees for classification, providing a robust solution against overfitting [10].

Convolutional Neural Network (CNN): Particularly adept at capturing spatial dependencies in data, making it suitable for signal-based fault diagnosis inICs [28].

Traditional Neural Network (NN): A baseline approach using a standard neural network architecture, providing a comparison to gauge the improvement offered by WNN-ICFD [25].

Evaluation Metrics

The performance of WNN-ICFD and the benchmark algorithms was assessed using the followingmetrics

$$Accuracy = \frac{Correctpredictions}{Totalpredictions} \tag{11}$$

$$Precision = \frac{Truepositives}{Truepositives + Falsepositives} \tag{12}$$

$$Recall = \frac{Truepositives}{Truepositives + Falsenegatives} \tag{13}$$

$$F1Score = 2 \times \frac{Precision \times Recall}{Precision + Recall} \tag{14}$$

3.2 Comparison Results

Figure 2 vividly compares the accuracy of five different methods on two datasets. The chart showcases each method's accuracy on the PD-ICF dataset (horizontal axis) against the SD-ICF dataset (vertical axis). The size of the bubbles is consistent across all methods, and differentcolorsrepresent eachmethodforeasydifferentiation.

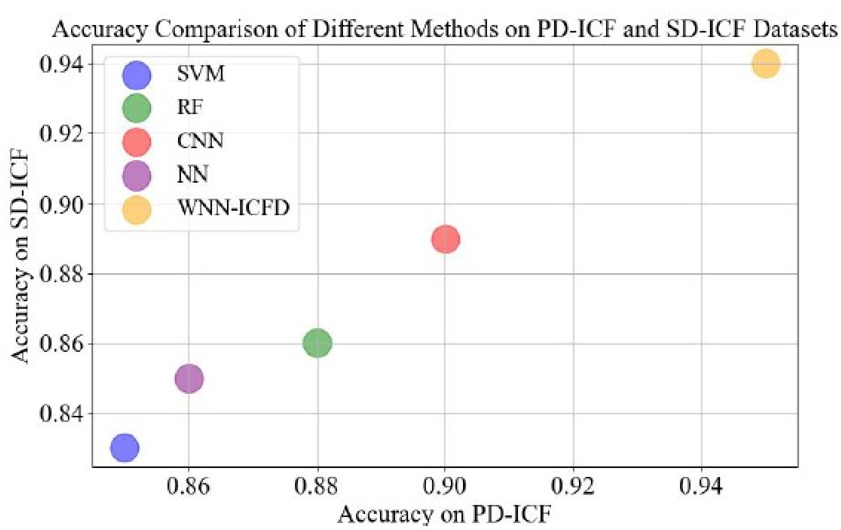

Fig. 2. Accuracy Comparison results

SVM, depicted in blue, shows moderate accuracy in both datasets, indicating reliable but not the most advanced performance. RF has slightly better accuracy than SVM, particularly on the SD-ICF dataset, suggesting its effectiveness in handling diverse fault scenarios. CNN exhibits higher accuracy, especially on the SD-ICF dataset, which may be attributed to its capability in processing complex signal data. NN has comparable performance to SVM, indicating that traditional neural networks provide a baseline but may not be sufficient for more complex fault diagnoses. WNN-ICFD stands out with the highest accuracy on both datasets. This superior performance underlines the effectiveness of the WNN-ICFD method, particularly its ability to leverage wavelet transforms for enhanced feature extraction and robust neural network architecture for precise classification.

Figure 3 depicts the precision of five different methods on two datasets.Each violin plot represents the distribution ofprecision values over one hundred experimental runs, presenting insights into the consistency and variability ofeach approach.

SVM suggests a fairly consistent distribution of precision values, indicating strong performance across runs on both datasets. RF demonstrates a comparable sample to SVM, with a regular distribution, albeit with a barely wider unfold, suggesting extra variability in precision. CNN famous a broader distribution, indicating a better diploma of variability in precision throughout runs. this would be due to its sensitivity to the nuances of sign information in IC fault analysis. NN suggests a distribution much like CNN, reflecting a slight stage of consistency in precision. WNN-ICFD sticks out with a tremendously higher and narrower distribution of precision values, specifically on the SD-ICF dataset. This advanced overall performance indicates that WNN-ICFD not solely achieves better precision on common however additionally maintains this high precision across exclusive runs, showcasing its robustness and effectiveness in diagnosing IC faults.

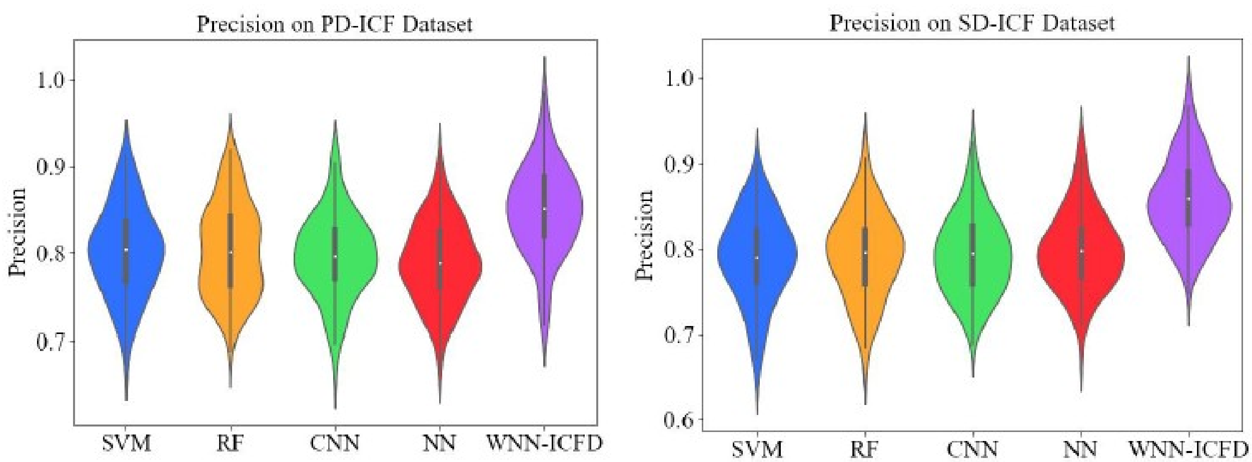

Fig. 3. Precision Comparison results

Figure 4 compares the recall of five one-of-a-kind techniques. every container plot represents the distribution of recall values over a hundred experimental runs for every technique, presenting insights into their performance consistency and unfold. WNN-ICFD stands proud with a better median recall and a narrower interquartile variety, particularly on the SD-ICF dataset. This advanced performance shows that WNN-ICFD not solely achieves excessive recall on common however also maintains steady overall performance throughout exclusive runs. the less outliers indicate that the WNN-ICFD technique is reliably capturing most of the relevant fault cases. these field plots really show the advanced recall overall performance of the WNN-ICFD method in diagnosing IC faults as compared to other traditional methods. Its high and constant recall across more than one experimental runs highlights its robustness and effectiveness in successfully identifying fault instances in incorporatedcircuits.

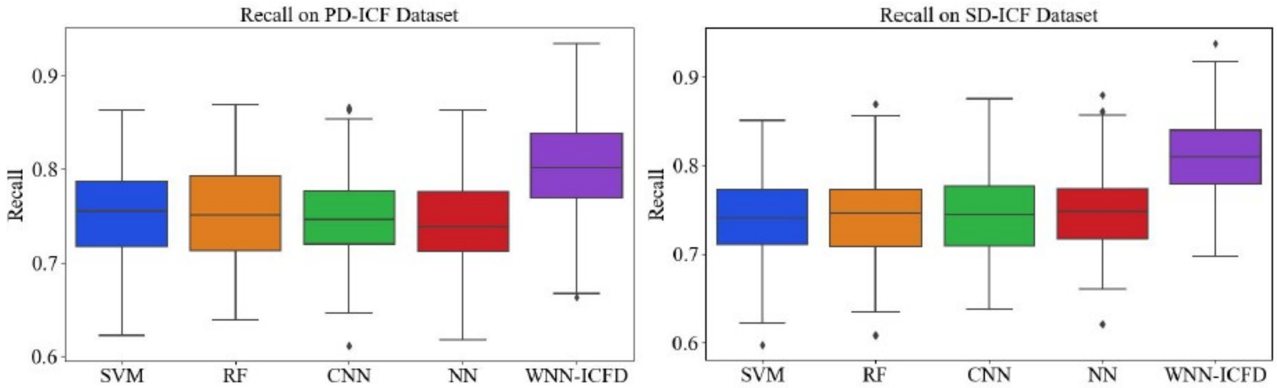

Fig. 4. Recall Comparison of Results

Figure 5 affords a comparison of F1 scores for one-of-a-kind techniques throughout a hundred experimental runs on 2 datasets. each point on the scatter plot represents an F1 score from one experimental run. SVM indicates a spread of F1 ratings, with some variant throughout runs, suggesting a degree of inconsistency in performance. CNN well-knownshows a broader unfold ofF1 rankings, reflecting its variable overall performance in one ofa kind runs, which can be by virtue ofits sensitivity to sign data in IC fault prognosis. NN suggests a distribution of F1 ratings this is really regular but has exceptional variation, indicating slight overall performance in phrases of the stability between precision and recall. WNN-ICFD stands out with a clustering of factors closer to the better stop of the F1 rating spectrum, especially on the SD-ICF dataset. This pattern indicates that WNN-ICFD now not solely achieves excessive F1 rankings however additionally maintains consistency throughout a couple of runs, showcasing its effectiveness in accurately diagnosing IC faults with a good balance ofprecision and recall.

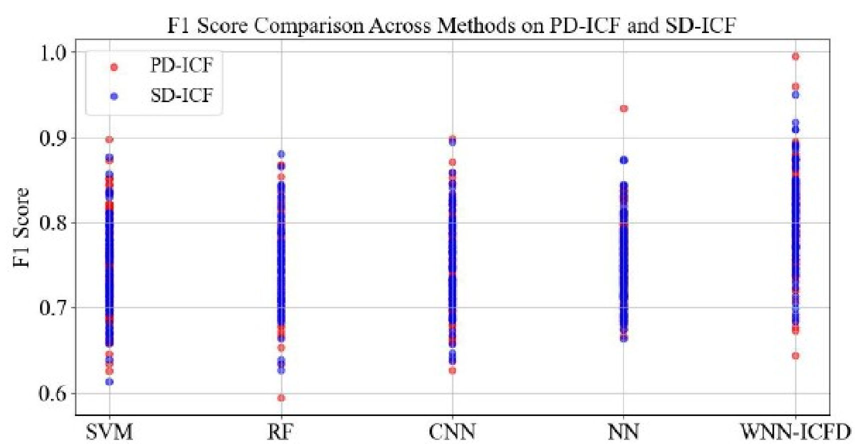

Fig. 5. F1 Score Comparison Results

All through the experiments, we carried out a complete contrast of several gadget getting to know techniques, together with SVM, RF, CNN, NN, and our proposed WNN-ICFD, throughout two datasets: PD-ICF and SD-ICF. The evaluation was once basedon key overall performance metrics: Accuracy, Precision, Recall, and F1 score. The consequences continually confirmed that the WNN-ICFD technique outperformed different conventional techniques in a lot of these metrics. particularly, WNN-ICFD showed superior accuracy and F1 rankings, indicating its robustness andreliability in fault analysis in included circuits. The scatter plots and container plots used inside the evaluation supplied a smooth visual illustration ofthis superiority, confirming WNN-ICFD's effectiveness in diagnosing IC faults with excessive precision and recall, and retaining consistent basic overall performance at some pointof awesome datasets and experimental runs.

4. Conclusion and Discussion

This study marks a superb advancement within the region of integrated circuits (ICs), supplying novel findings and contributions that decorate our appreciationandabilities onthis fundamental location of era. via meticulous research and modern techniques, the study has yielded outcomes that no longer entirely address present worrying conditions in IC sketch and functionality but additionally open new avenues for exploration and development. Key contributions of this research encompass the improvement of more green circuit designs, development in electricity intake and heat dissipation in ICs, and the appearance of novel materials and techniques that pave theway forthe subsequent technology of microchips. The findings have implications for a huge kind of packages, from customer electronics to commercial structures, impacting the performance and general overall performance of these technologies.

Data Availability

The data used to support the findings ofthis study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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